IN THE CLAIMS

Please amend the claims as set forth below:

1. (Currently Amended) An active-matrix display device comprising:

pixel circuits arrayed in a matrix;

signal lines each of which is interconnected with a corresponding column of the matrixarrayed pixel circuits; and

a first scanning line, a second scanning line, a third scanning line, and a fourth scanning line which that are interconnected with a corresponding row of the matrix-arrayed pixel circuits;

each of the pixel circuits comprising:

a first transistor of which a gate terminal is connected with the first scanning line and of which a first electrode terminal is connected with one of the signal lines;

a first capacitor of which a first end is connected with a second electrode terminal of the first transistor;

a second capacitor of which a first terminal is connected with the first end or a second end of the first capacitor;

a second transistor of which a gate terminal is connected with the second end of the first capacitor and of which a first electrode terminal is connected with a first power line;

a third transistor of which a gate terminal is connected with the second scanning line, a first electrode terminal of the third transistor is connected with the gate terminal of the second transistor, and a second electrode terminal of the third transistor is connected with a second electrode terminal of the second transistor;

a fourth transistor of which a gate terminal is connected with the third scanning line and of which a first electrode terminal is connected with the second electrode terminal of the second transistor;

a fifth transistor of which a gate terminal is connected with the fourth scanning line, a first electrode terminal of the fifth transistor is connected with a third power line, and a second electrode terminal of the fifth transistor is connected with the second electrode terminal of the first transistor; and

a display element connected with both a second electrode terminal of the fourth transistor and a second power line.

- 2. (Original) The active-matrix display device according to Claim 1, wherein the third transistor and the fifth transistor have the same conductivity type, and the second scanning line and the fourth scanning line are combined as a common line.
- 3. (Original) The active-matrix display device according to Claim 1, wherein the third transistor and the fourth transistor have opposite conductivity types, and the second scanning line and the third scanning line are combined as a common line.
- 4. (Original) The active-matrix display device according to Claim 1, wherein the fourth transistor and the fifth transistor have opposite conductivity types, and the third scanning line and the fourth scanning line are combined as a common line.
- 5. (Original) The active-matrix display device according to Claim 1, wherein the third transistor and the fifth transistor have a conductivity type opposite to that of the fourth transistor; and the second scanning line, the third scanning line, and the fourth scanning line are combined as a common line.
- 6. (Original) The active-matrix display device according to Claim 1, wherein the first power line and the third power line are combined as a common line.
- 7. (Original) The active-matrix display device according to Claim 1, wherein a power-supply voltage of the third power line is lower than that of the first power line.

8. (Original) The active-matrix display device according to Claim 7, wherein the power-supply voltage of the third power line is variable.

- 9. (Original) The active-matrix display device according to Claim 1, wherein the first to fifth transistors are polysilicon thin film transistors.
- 10. (Original) The active-matrix display device according to Claim 1, wherein the display element is an organic electroluminescent element which includes an organic layer having a luminous layer disposed between a first electrode and a second electrode.
- 11. (Currently Amended) A method for driving an active-matrix display device, the device comprising: pixel circuits arrayed in a matrix; signal lines each of which is interconnected with a corresponding column of the matrix-arrayed pixel circuits; and a first scanning line, a second scanning line, a third scanning line, and a fourth scanning line which that are interconnected with a corresponding row of the matrix-arrayed pixel circuits;

each of the pixel circuits comprising:

a first transistor of which a gate terminal is connected with the first scanning line and of which a first electrode terminal is connected with one of the signal lines; a first capacitor of which a first end is connected with a second electrode terminal of the first transistor; a second capacitor of which a first terminal is connected with the first end or a second end of the first capacitor; a second transistor of which a gate terminal is connected with the second end of the first capacitor and of which a first electrode terminal is connected with a first power line; a third transistor of which a gate terminal is connected with the second scanning line, a first electrode terminal of the third transistor is connected with the gate terminal of the second transistor, and a second electrode terminal of the third transistor is connected with a second electrode terminal of the second transistor; a fourth transistor of which a gate terminal is connected with the third scanning line and of which a first electrode terminal is connected with the second electrode terminal of the second transistor; a fifth transistor of which a gate terminal is connected with the fourth scanning line, a first electrode terminal of the fifth transistor is connected with a third power line, and a second electrode terminal of the fifth transistor is connected with the second electrode terminal of the fifth transistor is connected with the second electrode terminal of the fifth transistor is connected with the second electrode terminal of the fifth transistor is connected with the second electrode terminal of the fifth transistor is connected between a second

electrode terminal of the fourth transistor and a second power line; the method comprising the steps of:

turning the first transistor and the fourth transistor off while turning the third transistor and the fifth transistor on to compensate <u>for</u> a threshold voltage of the second transistor in each pixel; and

turning the first transistor on while turning the third transistor and the fifth transistor off to write display data into each pixel from the signal line.

12. (Currently Amended) The method for driving an active-matrix display device according to Claim 11, wherein a period for compensating the threshold voltage and a period for writing the display data reside simultaneously in pixels which that are in different rows and are connected along the same signal line.